WHAT IS CLAIMED IS:

1. A differential amplifier circuit comprising:

a low gain fully differential amplifier; and

a high gain fully differential amplifier connected in parallel with the low gain fully differential amplifier with a positive input of the low gain fully differential amplifier being connected to positive input of the high gain fully differential amplifier and connected to positive input of the circuit, with a negative input of the low gain fully differential amplifier being connected to negative input of the high gain fully differential amplifier and connected to negative input of the circuit, negative and positive outputs of the low gain fully differential amplifier being connected to positive and negative load terminals, respectively, of the high gain fully differential amplifier,

wherein negative and positive outputs of the high gain fully differential amplifier become negative and positive outputs, respectively, of the circuit, and

wherein when the low gain fully differential amplifier biases, the high gain fully differential amplifier, the positive and negative outputs of the circuit are stable during a common mode operation without being impacted by a fluctuation of the inputs.

2. The amplifier of claim 1 wherein the low gain fully differential amplifier further includes:

at least one current source coupled to first and second differential current paths for receiving the positive and negative inputs;

a first self-biased loading in the first current path controlled by the positive input for generating the negative output thereof as a first loading bias input of the high gain differential amplifier for generating the positive output of the circuit; and

a second self-biased loading in the second current path controlled by the negative input for generating the positive output thereof as a second loading bias input of the high gain differential amplifier for generating the negative output of the circuit.

3. The amplifier of claim 2 wherein the positive and negative inputs control the current paths by controlling gates of two pMOS transistors in the current paths.

4. The amplifier of claim 2 wherein the current source is a pMOS transistor connected to a supply voltage.

5. The amplifier of claim 2 wherein the low gain fully differential amplifier further includes a supplemental loading module for diverting current coming into the first and second differential current paths.

6. The amplifier of claim 5 wherein the supplemental loading module is an output level modification module with a current mirror type circuit sharing the current source with the two differential current paths for modifying levels of the positive and negative outputs.

7. The amplifier of claim 6 wherein the output level modification module has two nMOS transistors connected in parallel whose drains are connected to the current source.

8. The amplifier of claim 5 wherein the supplemental loading module is a gain improvement module for increasing the gain of the positive and negative outputs.

9. The amplifier of claim 8 wherein the gain improvement module has first and second nMOS transistors cross connected with each gate connected to the other's drain for sharing the current in the two differential current paths.

10. The amplifier of claim 1 wherein the high gain fully amplifier further includes:

at least one current source passing current along first and second differential current paths,

wherein the first differential current path having a first pMOS transistor with its gate controlled by the positive input and a first nMOS transistor connected in series with a gate thereof connected to the positive output of the low gain fully differential amplifier, and the second differential current path having a second pMOS transistor with its gate controlled by the negative input and a second nMOS transistor connected in series with a gate thereof connected to the negative output of the low gain fully differential amplifier,

wherein a drain of the second nMOS transistor generates the positive output of the circuit and a drain of the first nMOS transistor generates the negative output of the circuit.

11. The amplifier of claim 1 further comprising first and second output stage modules for the positive and negative outputs of the circuit for increasing an output swing and loading capacity.

12. The amplifier of claim 11 wherein the first and second output stage modules each has a pMOS transistor connected to a high voltage supply with its gate

controlled by a bias voltage, an nMOS transistor connected in series with the pMOS transistor with its gate controlled by the corresponding positive or negative output of the circuit, and a capacitor providing an AC coupling to pass the corresponding positive or negative output.

13. The amplifier of claim 1 wherein the low and high gain fully differential amplifiers share at least one current source coupled to first and second differential current paths of both the low and high gain fully differential amplifiers.

14. The amplifier of claim 13 wherein the low gain fully differential amplifier further includes:

a first self-biased loading in the first current path controlled by the positive input for generating the negative output thereof as a first loading bias input of the high gain differential amplifier for generating the positive output of the circuit; and

a second self-biased loading in the second current path controlled by the negative input for generating the positive output thereof as a second loading bias input of the high gain differential amplifier for generating the negative output of the circuit.

15. The amplifier of claim 13 wherein the positive and negative inputs control the current paths by controlling gates of two pMOS transistors in the current paths.

16. The amplifier of claim 13 wherein the low gain fully differential amplifier further includes a supplemental loading module for diverting current coming into the first and second differential current paths.

17. The amplifier of claim 13 wherein the first differential current path in the high gain fully amplifier has a first pMOS transistor with its gate controlled by the positive input and a first nMOS transistor connected in series with a gate thereof connected to the positive output of the low gain fully differential amplifier, and wherein the second differential current path has a second pMOS transistor with its gate controlled by the negative input and a second nMOS transistor connected in series with a gate thereof connected to the negative output of the low gain fully differential amplifier,

wherein a drain of the second nMOS transistor generates the positive output of the circuit and a drain of the first nMOS transistor generates the negative output of the circuit.

18. The amplifier of claim 13 further comprising first and second output stage modules for the positive and negative outputs of the circuit for increasing an output swing and loading capacity.

19. A complementary metal-oxide-semiconductor (CMOS) fully differential amplifier comprising:

a low gain fully differential amplifier having a first pMOS transistor passing a current on first and second differential current paths when controlled by a bias voltage, each differential current path having pMOS transistor and a nMOS transistor connected in series, the first differential current path having a second pMOS transistor controlled by a first input and a first self-biased nMOS transistor whose gate and drain being connected to produce a first low gain bias output and the second differential current path having a third pMOS transistor controlled by a second input and a second self-biased nMOS transistor whose gate and drain being

connected to produce a second low gain bias output; and

a high gain fully differential amplifier connected in parallel with the low gain fully differential amplifier having a fourth pMOS transistor passing the current on third and fourth differential current paths when controlled by the bias voltage, the third differential current path having a fifth pMOS transistor with its gate controlled by the first input and a third nMOS transistor connected in series with a gate thereof connected to the second low gain bias output, and the fourth differential current path having a sixth pMOS transistor with its gate controlled by the second input and fourth nMOS transistor connected in a series with a gate thereof connected to the first low gain bias output,

wherein a first output is generated at a drain of the fourth nMOS transistor and a second output is generated at a drain of the third nMOS transistor,

wherein the low gain fully differential amplifier biases the high gain fully differential amplifier through the first and second low gain bias outputs so that the first and second outputs are stable during a common mode operation without being impacted by a fluctuation of the inputs.

20. The amplifier of claim 19 wherein the low gain fully differential amplifier further includes a supplemental loading module for diverting current coming into the first and second differential current paths.

21. The amplifier of claim 20 wherein the supplemental loading module is an output level modification module with a current mirror type circuit sharing the current with the first and second differential current paths for modifying levels of the first and second outputs.

22. The amplifier of claim 21 wherein the output level modification module has two nMOS transistors connected in parallel whose drains are connected to the drain of the first pMOS transistor.

23. The amplifier of claim 20 wherein the supplemental loading module is a gain improvement module for increasing the gain of the first and second outputs.

24. The amplifier of claim 23 wherein the gain improvement module has fifth and sixth nMOS transistors cross connected with each gate connected to the other's drain, and with the drains of the second and fifth nMOS transistors connected together and the drains of the first and sixth nMOS transistors connected together, a transconductance of the first nMOS transistor being larger than that of the sixth nMOS transistor and a transconductance of the second nMOS transistor being larger than that of the fifth nMOS transistor.

25. The amplifier of claim 21 further comprising first and second output stage modules connected to the first and second outputs for increasing an output swing and loading capacity.

26. The amplifier of claim 24 wherein the first and second output stage modules each has a pMOS transistor connected to a high voltage supply with its gate controlled by the bias voltage, an nMOS transistor connected in series with the pMOS transistor with its gate controlled by the corresponding first or second output, and a capacitor providing a phase compensation thereof.

27. A complementary metal-oxide-semiconductor (CMOS) fully differential

amplifier comprising:

a low gain fully differential amplifier having a first pMOS transistor passing a current on first and second differential current paths when controlled by a bias voltage, each differential current path having a pMOS transistor and nMOS transistors connected in series, the first differential current path having a second pMOS transistor controlled by a first input and a first self-biased nMOS transistor whose gate and drain being connected to produce a first low gain bias output and the second differential current path having a third pMOS transistor controlled by a second input and a second self-biased nMOS transistor whose gate and drain being connected to produce a second low gain bias output; and

a high gain fully differential amplifier connected in parallel with the low gain fully differential amplifier having a fourth pMOS transistor passing the current on third and fourth differential current paths when controlled by the bias voltage, the third differential current path having a fifth pMOS transistor with its gate controlled by the first input and a third nMOS transistor connected in series with a gate thereof connected to the second low gain bias output, and the fourth differential current path having a sixth pMOS transistor with its gate controlled by the second input and fourth nMOS transistor connected in series with a gate thereof connected to the first low gain bias output; and

wherein a first output is generated at a drain of the fourth nMOS transistor and a second output is generated at a drain of the third nMOS transistor,

wherein the low gain fully differential amplifier biases the high gain fully differential amplifier through the first and second low gain bias outputs so that the first and second outputs are stable during a common mode operation without being impacted by a fluctuation of the inputs, and

wherein first and second output stage modules are connected to the first and

second outputs for increasing an output swing and loading capacity.

28. The amplifier of claim 20 wherein the low gain fully differential amplifier further includes a current mirror type circuit sharing the current with the first and second differential current paths for modifying levels of the first and second outputs.

29. The amplifier of claim 20 wherein the low gain fully differential amplifier further includes a gain improvement module for increasing the gain of the first and second outputs.

30. The amplifier of claim 22 wherein the gain improvement module has fifth and sixth nMOS transistors cross connected with each gate connected to the other's drain, and with the drains of the second and fifth nMOS transistors connected together and the drains of the first and sixth nMOS transistors connected together, a transconductance of the first nMOS transistor being larger than that of the sixth nMOS transistor and a transconductance of the second nMOS transistor being larger than that of the fifth nMOS transistor.

31. The amplifier of claim 20 wherein the first and second output stage modules each has a pMOS transistor connected to a high voltage supply with its gate controlled by the bias voltage, an nMOS transistor connected in series with the pMOS transistor with its gate controlled by the corresponding first or second output, and a capacitor providing a phase compensation thereof.

32. A low voltage complementary metal-oxide-semiconductor (CMOS)

differential amplifier comprising:

a low gain fully differential amplifier passing a current on first and second differential current paths, each differential current path having a pMOS transistor and nMOS transistors connected in series, the first differential current path having a first pMOS transistor controlled by a first input and a first self-biased nMOS transistor whose gate and drain being connected to produce a first low gain bias output and the second differential current path having a second pMOS transistor controlled by a second input and a second self-biased nMOS transistor whose gate and drain being connected to produce a second low gain bias output; and

a high gain fully differential amplifier connected in parallel with the low gain fully differential amplifier passing the current on a third and fourth differential current path, the third differential current path having a third pMOS transistor with its gate controlled by the first input and a third nMOS transistor connected in series with a gate thereof connected to the second low gain bias output, and the fourth differential current path having a fourth pMOS transistor with its gate controlled by the second input and fourth nMOS transistor connected in series with a gate thereof connected to the first low gain bias output,

wherein the pMOS transistors are coupled to a predetermined low voltage supply,

wherein a first output is generated at a drain of the fourth nMOS transistor and a second output is generated at a drain of the third nMOS transistor, and

wherein the low gain fully differential amplifier biases the high gain fully differential amplifier through the first and second low gain bias outputs so that the first and second outputs are stable during a common mode operation without being impacted by a fluctuation of the inputs.

33. The amplifier of claim 25 wherein the low gain fully differential amplifier further includes:

a first self-biased loading in the first current path controlled by the positive input for generating the negative output thereof as a first loading bias input of the high gain differential amplifier for generating the positive output of the circuit; and

a second self-biased loading in the second current path controlled by the negative input for generating the positive output thereof as a second loading bias input of the high gain differential amplifier for generating the negative output of the circuit.

34. The amplifier of claim 26 wherein the low gain fully differential amplifier further includes a supplemental loading module for diverting current coming into the first and second differential current paths.

35. The amplifier of claim 27 wherein the supplemental loading module is an output level modification module with a current mirror type circuit sharing the current source with the two differential current paths for modifying levels of the positive and negative outputs.

36. The amplifier of claim 27 wherein the supplemental loading module is a gain improvement module for increasing the gain of the positive and negative outputs.

37. The amplifier of claim 25 wherein the first differential current path of the high gain fully differential amplifier has a first pMOS transistor with its gate controlled by the positive input and a first nMOS transistor connected in series with a gate thereof connected to the positive output of the low gain fully differential amplifier,

and wherein the second differential current path has a second pMOS transistor with its gate controlled by the negative input and a second nMOS transistor connected in series with a gate thereof connected to the negative output of the low gain fully differential amplifier,

wherein a drain of the second nMOS transistor generates the positive output of the circuit and a drain of the first nMOS transistor generates the negative output of the circuit.

38. The amplifier of claim 25 further comprising a first and second output stage module for the positive and negative outputs of the circuit for increasing an output swing and loading capacity.